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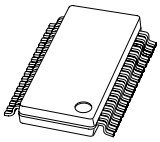

AN10495

HDMI, DVI interface protection

Rev. 01 — 18 December 2007 **Application note**

Document information

Info	Content
Keywords	DVI, HDMI, DDC, CEC, Hot-Plug, level shifting, ESD, backdrive protection
Abstract	This application note gives an overview about the importance and various opportunities for sophisticated ESD protection for HDMI receiver and transmitter interfaces. A broad portfolio of interface solutions starting from pure ESD protection arrays up to fully integrated interface ICs including level shifting, ESD and backdrive protection are discussed. Important TDR measurements as well as Eye diagrams demonstrate the high performance of these NXP Semiconductors products with the world-wide lowest line capacitance available in Silicon technology. It is demonstrated, that such fully integrated solutions from NXP Semiconductors enables easy routing and relaxed board design. The presented solutions are fully compliant with HDMI 1.2 and HDMI 1.3.

Revision history

Rev	Date	Description
01	20071218	Initial version

Contact information

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1. Introduction

The High Definition Multimedia Interface (HDMI) is the state-of-the-art interface combining the video and audio signals into a single digital interface for use with Digital Versatile Disc (DVD) players, Digital TeleVisions (DTVs), Set-Top Boxes (STBs), game consoles and other audiovisual devices.

HDMI is a merge of:

- DVI for the TMDS interface (mainly single link)
- IEC 60958 and IEC 61937 for the audio
- EIA/CEA-861B for video timing and auxiliary information

HDMI supports standard, enhanced or high-definition video signals plus standard to multi-channel surround-sound audio, and HDCP copy protection. It ensures that the HDMI source is using video and audio formats (such as EDID) which are supported by the HDMI sink. HDMI includes uncompressed digital video, a high bandwidth in the gigabytes-per-second range, one connector instead of several cables and connectors, and communication between the video source and the receiver e.g. a TV set.

The HDMI Founders group includes the leading consumer electronics manufacturers Hitachi, Matsushita Electric Industrial, Philips, Sony, Thomson, Toshiba, and Silicon Image. Digital Content Protection, LLC (a subsidiary of Intel) is providing High-bandwidth Digital Content Protection (HDCP) for HDMI. In addition, HDMI has the support of major motion picture producers Fox, Universal, Warner Bros. and Disney, and system operators DirecTV, EchoStar as well as CableLabs.

The HDMI Founders group has established Authorized Testing Centers (ATC) where licensed manufacturers can submit their products for HDMI compliance testing. Currently, ATCs are located at Matsushita Electric Industrial in Japan, NXP Semiconductors in France (Caen), and Silicon Image in USA.

Both HDMI receiver and HDMI transceiver ICs are manufactured in processes with deep sub-micron feature sizes. These sensitive sub-micron CMOS processes typically provide a limited 2 kV ESD protection according to the Human Body Model (HBM, MIL-883E method 3015.7/JESD22-A114-D) standard in order to provide protection during the manufacturing and assembly process. An end-user application such as a TV or Set Top Box (STB) encounters a high risk of ESD damage, which is specifically high for Hot-Plug interfaces such as HDMI. In these Hot-Plug interfaces, the consumer can plug or unplug cables while the application is running. Furthermore, most manufacturers seek to get certain consumer electronics certificates (e.g. CE norm), which do require high-level ESD protection according to the IEC 61000-4-2 standard.

In the above cases, all manufacturers strongly recommend applying ESD protection circuitry at their external port interface. NXP Semiconductors has developed a broad range of DVI/HDMI interface ICs which not only provide high-level ESD protection, but also incorporate level shifting for the DDC signals and provide backdrive protection functionality. Such ICs are essential for a high-speed DVI/HDMI port with data rates in the GHz range.

For ESD protection, NXP Semiconductors offers a broad variety of solutions such as a 4-channel pure ESD protection solution device (IP4280CZ10) as well as a fully integrated interface IC including ESD protection, level shifting and backdrive protection device

(IP4776CZ38). Depending on the specific HDMI transmitter and the customer choice, any of these solutions can be applied. Based on current experience, NXP Semiconductors recommends the higher integrated solutions in order to obtain easier routing, relaxed board layout, smallest footprints and highest ESD protection level.

This report is structured as follows.

Section 2 gives an overview and a short description of the relevant ESD protection standards. A special rail-to-rail-based diode concept, as used by NXP Semiconductors to achieve ultra-low line capacitance for high-speed data interface, is discussed in Section 3. Section 4 gives a brief explanation of level shifting and Section 5 discusses backdrive protection required at some HDMI ports. In Section 6 an application for ESD protection without level shifting is drawn. Some basic information about Printed-Circuit Board (PCB) design is documented in Section 7. Section 8 introduces various ESD protection solutions for DVI/HDMI ports, starting from pure protection functionality up to a fully integrated interface IC. This section also includes all relevant HDMI compliance tests such as TDR (Time Domain Reflection) or Eye patterns proving the high performance of the NXP Semiconductors high-speed ESD protection devices. Section 9 ends this application note with a brief summary.

2. ESD protection standards

2.1 IEC 61000-4-2

Interfaces of consumer electronic equipment are widely specified according to the International Electrotechnical Commission standard IEC 61000-4-2. This standard is not targeted towards particular devices but towards general equipment, systems and subsystems that may be involved in electrostatic discharge. The model, shown in Figure 1, consists of a 150 pF capacitor and a 330 Ω series resistor representing the counterpart to the Device Under Test (DUT).

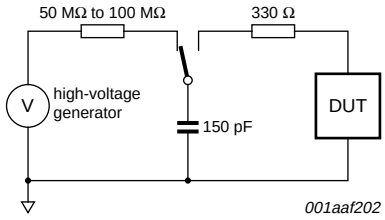


Fig 1. Test circuit according IEC 61000-4-2

According to this standard, the ESD surge can be applied by contact as well as by air discharge and is classified by the capacitor's charge voltage shown in Table 1.

For consumer products, class 4 is regarded as being the most appropriate level to achieve a reasonable relation between cost and prevention of field returns due to ESD failures.

Table 1. IEC 61000-4-2 ESD surge classification[1]

Contact discharge			Air discharge	
Class	**Test voltage (kV)**	**Maximum current (A)**	**Class**	**Test voltage (kV)**
1	2	7.5	1	2
2	4	15	2	4
3	6	22.5	3	8
4	8	30	4	15
X	special	special	X	special

[1] X is an open level that must be specified in the dedicated device specification. If higher voltages than level 4 are specified, special test equipment may be needed.

A typical ESD current pulse form generated by an ESD surge according to IEC 61000-4-2 shown in Figure 2.

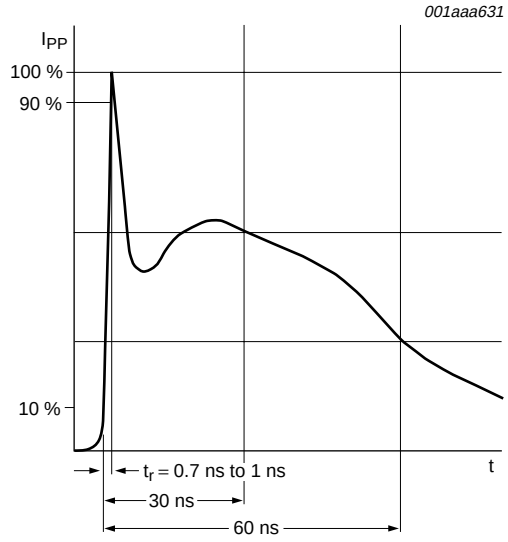


Fig 2. ESD surge according IEC 61000-4-2

A characteristic of IEC 61000-4-2 ESD pulses is the very short rising edge; the maximum peak current is reached within 0.7 ns to 1 ns. This requires a very short reaction time of the ESD protection circuit to avoid severe voltage overshoots at the protected device. Therefore, it is important to put special attention to the selection of the correct diodes. Ultra-low line capacitance diodes are the recommended device of choice, especially for high-speed interfaces such as HDMI, as they react very fast (in the nano second range).

Another issue besides the voltage clamping is the maximum current injected into a device during an ESD discharge. To withstand a maximum possible current of 30 A as specified in IEC 61000-4-2, level 4, careful dimensioning of all conductors and components affected by an ESD surge is mandatory. Using appropriate structural dimensions helps to obtain very short reaction times of the ESD protection circuits avoiding permanent damage caused by for example, electro-migration of aluminum tracks.

2.2 Human Body Model (HBM, MIL-883E method 3015.7)

The HBM standard simulates an ESD surge generated by human contact to electronic components.

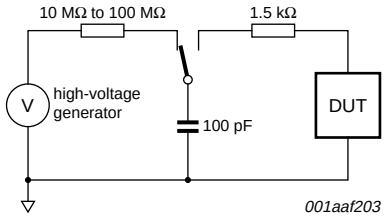


Fig 3. Test circuit according to MIL-883E method 3015.7

As shown in Figure 3, the model consists of a 100 pF capacitor and a 1.5 kΩ serial resistor to simulate a human body. According to the standard, the ESD surge is applied by contact and the test is applied in both the positive and negative direction. Three different classes differentiated by the capacitor's charge voltage are shown in Table 2.

Table 2. MIL-883E method 3015.7 ESD surge classification, contact discharge

Class	Test voltage (V)	Maximum current (A)
1	0 to 1999	1.33
2	2000 to 3999	2.67
3	4000 and above	> 2.67

A typical ESD current pulse form generated by an ESD surge according to MIL-883E method 3015.7 is shown in Figure 4.

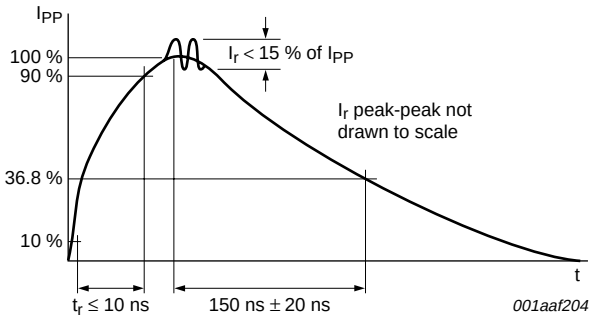


Fig 4. ESD surge according to MIL-883E method 3015.7

The shape of the ESD surge looks similar to an RC-charge/-discharge curve. As the maximum current applied is in the order of magnitude of a few amperes only, and the rise time is a few nanoseconds, the reaction time of an ESD protection circuit is relatively not critical.

2.3 Comparison of IEC and MIL standard

Direct comparison of both ESD models is difficult due to the differences in the discharge waveforms. Generally, the maximum injected current and the total load of the IEC 61000-4-2 standard is much higher than the one specified in the Human Body Model (HBM) according to the MIL-883E method 3015.7.

The rise time of the current waveform is different due to the series resistor being 1.5 kΩ in the HBM instead of 330 Ω as in the IEC 61000 model.

While the rise time for the IEC-compliant current waveform is specified as being 0.7 ns to 1 ns, the HBM waveform is specified as having a rise time below 10 ns only.

Assuming that the maximum current rating is more stressful to a protection ESD diode and other affected components than the duration of the current flow, the IEC 61000-4-2 standard is the more stringent of the two tests to withstand.

As the surge current is determined by the gradient of charge over time $I = \frac{\partial Q}{\partial t}$, the voltage drop across the protection diode can be described as being $V \approx R_{intrinsic} \times \frac{\partial Q}{\partial t}$, where $R_{intrinsic}$ is the inner resistance of the diode.

Looking at the likelihood of voltage overshoots being attributable to the rise time of ESD surges, one can easily derive, that shorter rise times will lead to higher voltage overshoots due to the reaction time of the respective protection devices. Even if, for instance, the test voltage of both methods is similar, the IEC standard is the more stringent test for a protection circuit to withstand because the maximum internal voltage will reach a higher level during a discharge.

In the case of the higher resistor value in the HBM, the maximum current would be in the order of some amperes only. In comparison to this, the maximum current of an ESD surge according to IEC can reach as high as 30 A.

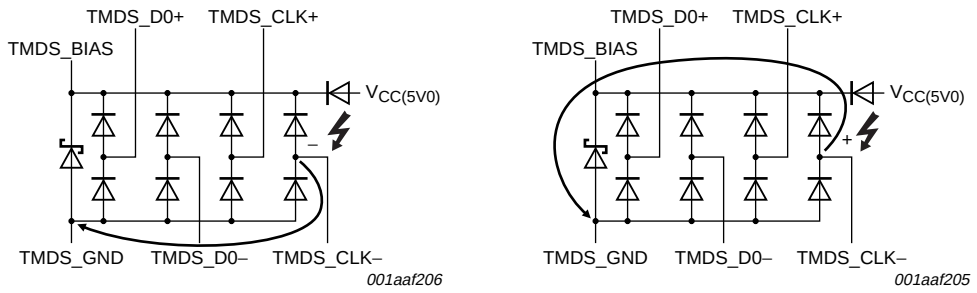
While integrated components such as resistors and also integrated planar aluminum metal wires have a limited maximum current density to avoid degradation effects such as, for example, electro-migration, certain design rules have to be maintained. High current densities might also result in a too high thermal stress in resistors and lead to a permanent shift of resistance value.

Both topics, electro-migration and thermal stress, are taken into account during our standard design procedure to avoid failure during a nearly unlimited number of ESD surges below the maximum voltage limit specified.

3. Rail-to-rail concept

With the rail-to-rail concept, a negative ESD strike on the I/O pin will cause one rail-to-rail diode (the lower diode at the flash sign in Figure 5a) to become forward biased, thereby transferring the ESD strike through the lower diode to ground.

A positive discharge strike will cause the other rail-to-rail diode (the upper diode at the flash sign in Figure 5b) to become forward biased transferring the discharge to the V_{CC} pin of the device. To prevent charging of the supply, the additional Zener diode between ground and V_{CC} will clamp voltages exceeding the Zener clamping voltage caused by the ESD strike to ground.



a. Negative ESD strike

b. Positive ESD strike

Fig 5. Rail-to-rail diode concept as used by NXP Semiconductors achieves ultra-low line capacitance

4. Level shifting

The new generation CMOS devices cannot handle high supply voltages which are specified in the DVI and HDMI specification. The typical core voltage of such a DVI/HDMI device is 1.8 V and the I/O cells are 3.3 V tolerant (GPIO, I^2C-bus). The IP4776CZ38 provides a 3.3 V to 5.0 V bidirectional level shifting between the DVI/HDMI transmitter/receiver chip and the HDMI plug. The implemented level shifter can also handle lower voltages like 3.3 V to support HDMI devices which are less tolerant.

In addition to the level shifting functionality as shown in Figure 6, an external pull-up resistor is needed to enable level shifting.

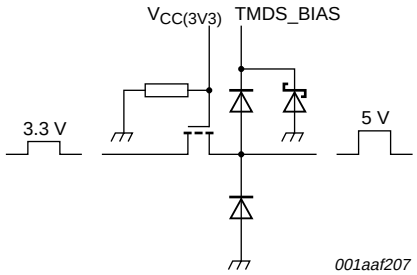


Fig 6. Principles of I^2C-bus level shifter

The NMOS FET, used in the level shifter is connected at the gate to the lower supply voltage (3.3 V).

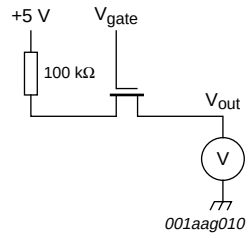


Fig 7. Measurements of I²C-bus level shifter

The output voltage at the low voltage side is $V_{gate(3.3V)} - V_{th}$. To reach the full 3.3 V high level voltage an additional pull-up resistor is needed. For signals like Hot-Plug the output voltage is high enough (about 2.4 V) to reach the logic level (2.0 V) and an additional pull-up resistor is not necessary.

The differential voltage between the gate and the low-level output is not constant. The voltage difference is increasing with the gate voltage as shown in Figure 8.

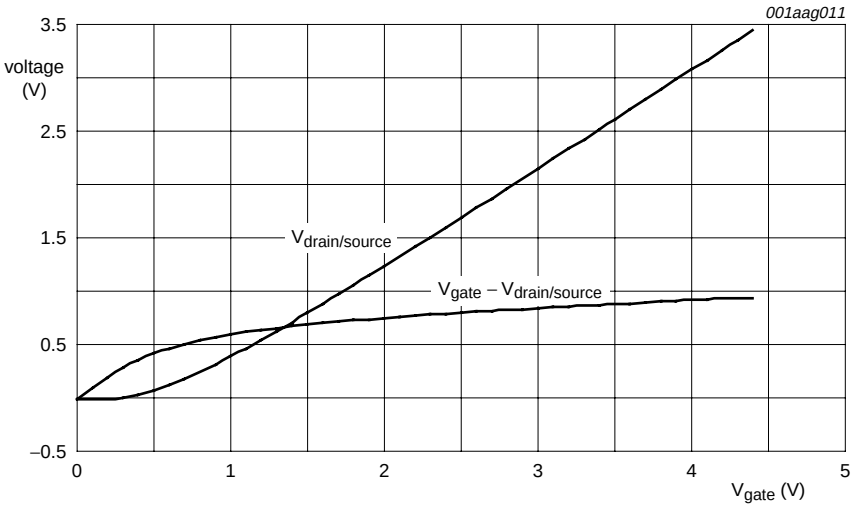


Fig 8. Output difference voltage at level shifter

The line $V_{drain/source}$ shows the output voltage at the low-level side (3.3 V). A minimum gate voltage V_{gate} is needed to produce an output voltage. The line $V_{gate} - V_{drain/source}$ shows the difference between the gate voltage and the output voltage.

If the supply voltage V_{gate} is 0 V, e.g. at power-down, the FET is high ohmic and therefore disconnects the input from the output. This is the mentioned backdrive protection that ensures that a switched-off device like a TV set is not pulling down any CEC, DDC or Hot-Plug signal.

4.1 DDC bus level shifting

The HDMI specification requires a pull-down resistor R_p of 1.5 kΩ to 2.2 kΩ for an HDMI source, 47 kΩ for an HDMI sink and a voltage of 5 V. The load of a cable (C_{cable}) is specified with a maximum value of 700 pF. The capacitive load of the HDMI sink and source is specified as 50 pF. The new CMOS technologies support lower voltages and today the maximum voltage at a pin is 3.3 V or less. Such a device requires a level shift function.

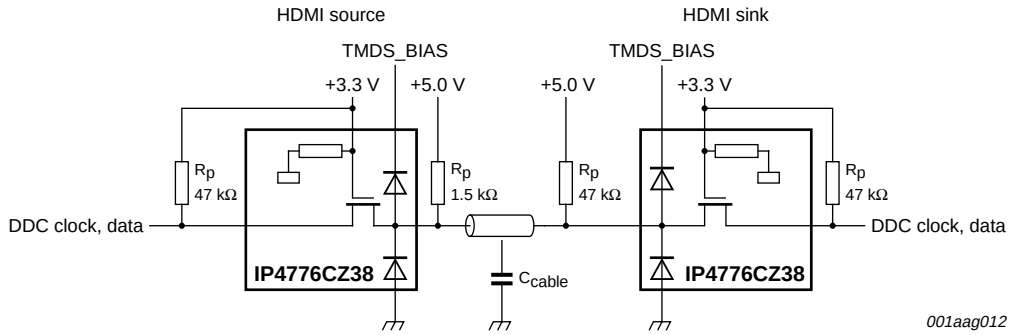


Fig 9. DDC application with level shift to 3.3 V and ESD protection

For devices without any need for level shifting, the level shifting function can be disabled by shorting the input and output pins of the device. The ESD protection continues to operate.

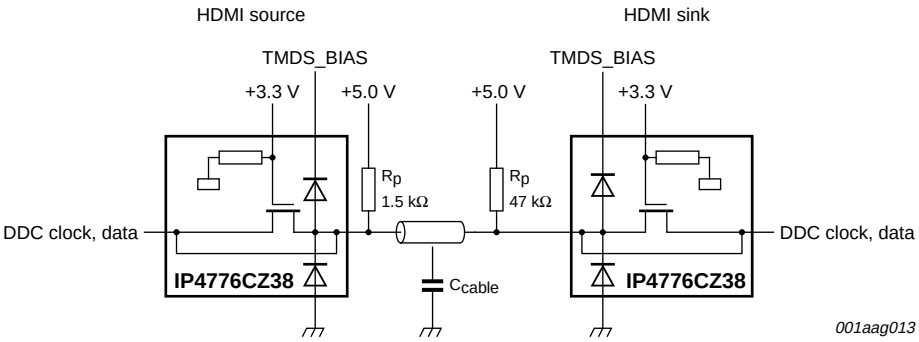


Fig 10. DDC application with ESD protection

The short can also be realized by a 0 Ω (zero Ohm) resistor on the PCB. This short also disables the backdrive protection. To keep the timing on the DDC lines synchronous we recommend using a 47 kΩ resistor for the DDC clock and the DDC data at the HDMI sink (start, stop condition detecting).

4.2 CEC bus

The single line CEC bus is working with a maximum signal voltage of 3.63 V at 1 kHz clock speed. Still the level shifting function in combination with backdrive protection can be used to adapt and protect the signal to a low-voltage DVI or HDMI input pin of a transmitter or receiver device.

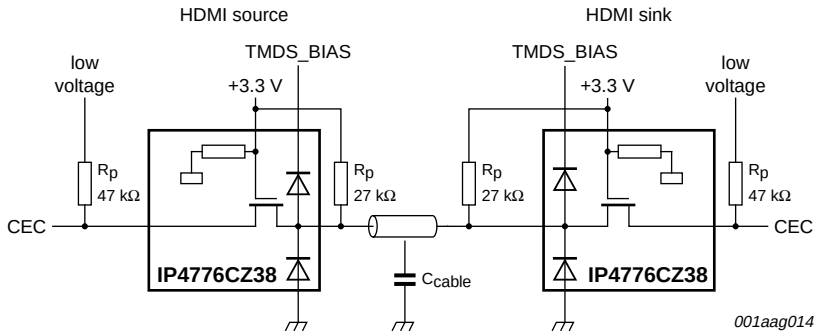


Fig 11. CEC application with level shift to low voltage and ESD protection

If backdrive protection and level shift function are not required, they can be disabled by shorting the input and output pins of the device so that only the ESD protection is used.

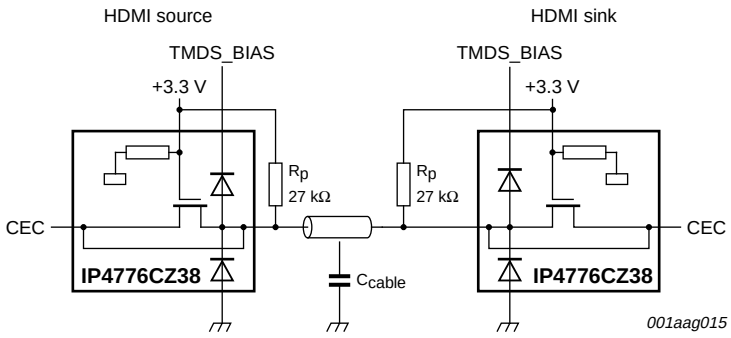


Fig 12. CEC application with ESD protection

4.3 Hot-Plug application

The Hot-Plug signal is used to control the communication between an HDMI sink and an HDMI source. The HDMI sink, for example a TV set, can pull down the Hot-Plug signal to a logic 0 as long as the sink is not ready for operation e.g. at system start-up.

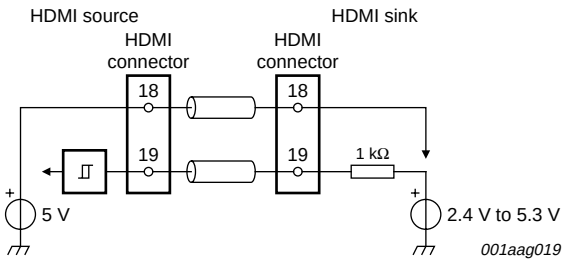


Fig 13. Principles of the Hot-Plug signal

The HDMI source uses a 2 V level to detect the Hot-Plug signal. The 5 V of the HDMI source or an internal voltage is used to generate the Hot-Plug signal via a 1 kΩ resistor (R_i).

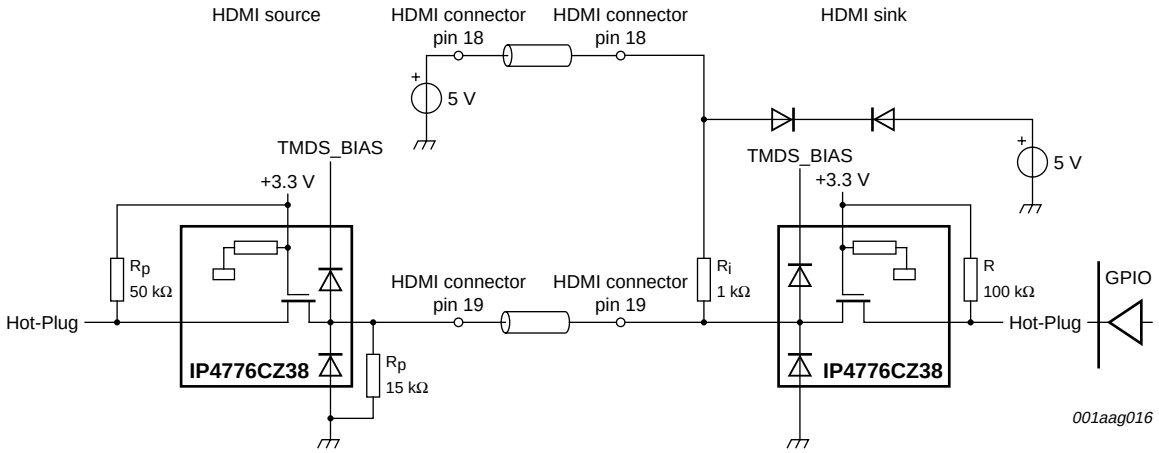


Fig 14. Hot-Plug, level shift and backdrive protection

The R_p of 50 kΩ can be removed because 2.4 V will be reached at the Hot-Plug out if the gate of the transistor is connected to 3.3 V. The combination of the pull-up resistors of 50 kΩ and 15 kΩ has the disadvantage that the low level (0.76 V) is close to the limit (0.8 V).

5. Backdrive protection

External signals can cause backdrive problems, particularly on output signals with pull-ups at the other end of the cable. I²C-bus signals like DDC clock, DDC data and the CEC lines can cause a potential problem on the DVI/HDMI source and sink side. Advanced sub-micron CMOS technology-based ICs, such as DVI/HDMI transceivers, are designed to have a typical internal 2 kV HBM ESD protection, intended to allow safe IC handling during the manufacturing process. These internal ESD diodes can create a direct path to ground so that pull-ups on the other end of the cable will sink current into the local, switched-off, TMDS_BIAS rail. Severe damage can be caused to unprotected sub-micron CMOS HDMI receiver and/or transmitter ICs, if for instance a non-standard DVI/HDMI adapter is used or two sinks/sources driving a DVI/HDMI source are plugged into each other. These configurations possibly might cause actual damage to the unprotected design. An external interface protection and isolation device, like the IP4776CZ38, will usually consume most of the energy and so protect the much more sensitive DVI/HDMI IC. To prevent these situations, the IP4776CZ38 contains an integrated backdrive protection that guarantees a maximum current of 5 µA on any I/O pin if the I/O pin voltage is higher than the supply voltage of the IP4776CZ38.

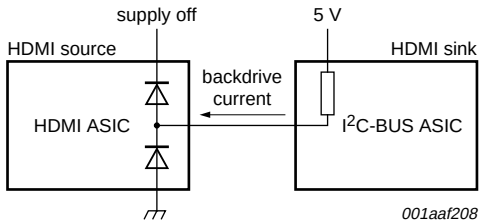


Fig 15. Principles of backdrive protection

Figure 15 shows the path of the current when the HDMI source is switched off and the HDMI sink is still active. The ESD diodes of the HDMI source device can create a short for signals at the HDMI cable.

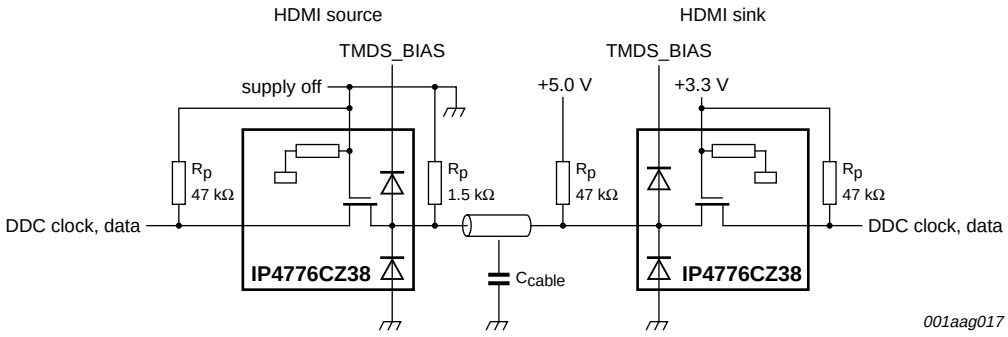


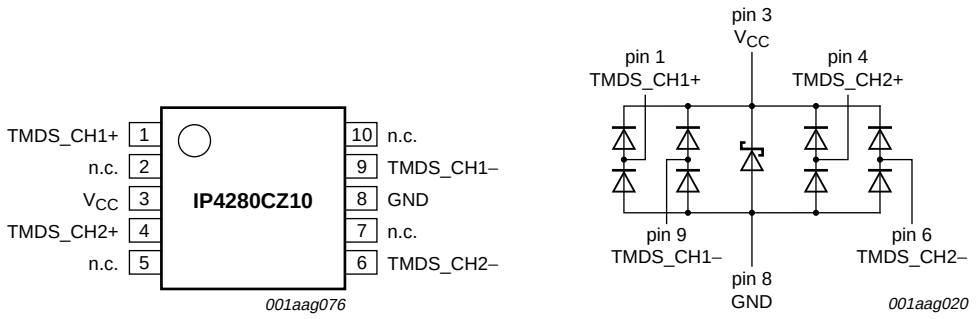
Fig 16. Backdrive protection at DDC bus

The level shift FET is high ohmic at power-down, preventing any backdrive current.

6. ESD protection of HDMI transceivers not requiring level shifting

Depending on the application, level shifting and/or backdrive protection might not be necessary for the DVI/HDMI interface. NXP Semiconductors provide a solution that offer the required high ESD protection (IEC 61000-4-2 level 4) combined with an ultra-low line capacitance.

Appropriate ESD protection using only a single chip is offered by the new generation ultra-low line capacitance diodes of the IP4280CZ10. This device is characterized by a line capacitance of only 0.7 pF, providing excellent protection, lowest capacitive load to the system and optimized parallel routing.



a. Pin allocation

b. Ultra-low line capacitance diodes

Fig 17. IP4280CZ10

Using the IP4776CZ38 including the level shifting feature but in a configuration in which level shifting is deactivated (by 5 V to the $V_{CC(3V3)}$ pin), the backdrive protection and the ESD protection are supported for DDC, CEC and Hot-Plug.

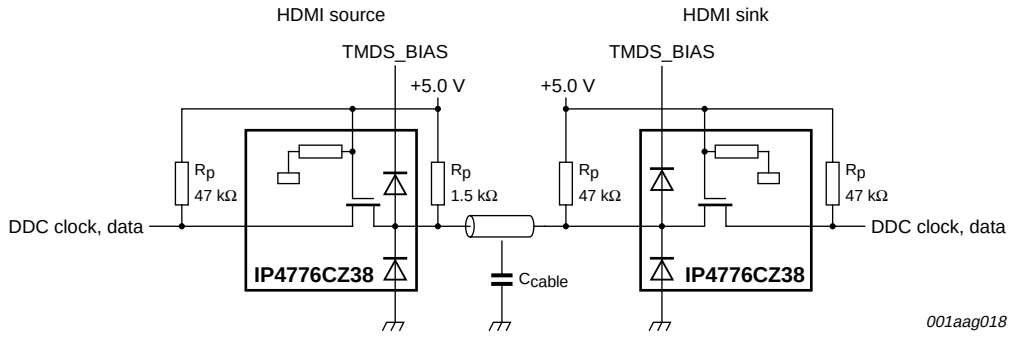


Fig 18. IP4776CZ38 with ESD and backdrive protection

7. PCB design

The design of the TMDS lines with respect to the impedance required by the HDMI specification (85 Ω to 115 Ω) requires detailed knowledge of the PCB materials used and the geometrical design of the Micro Strip Lines (MSL).

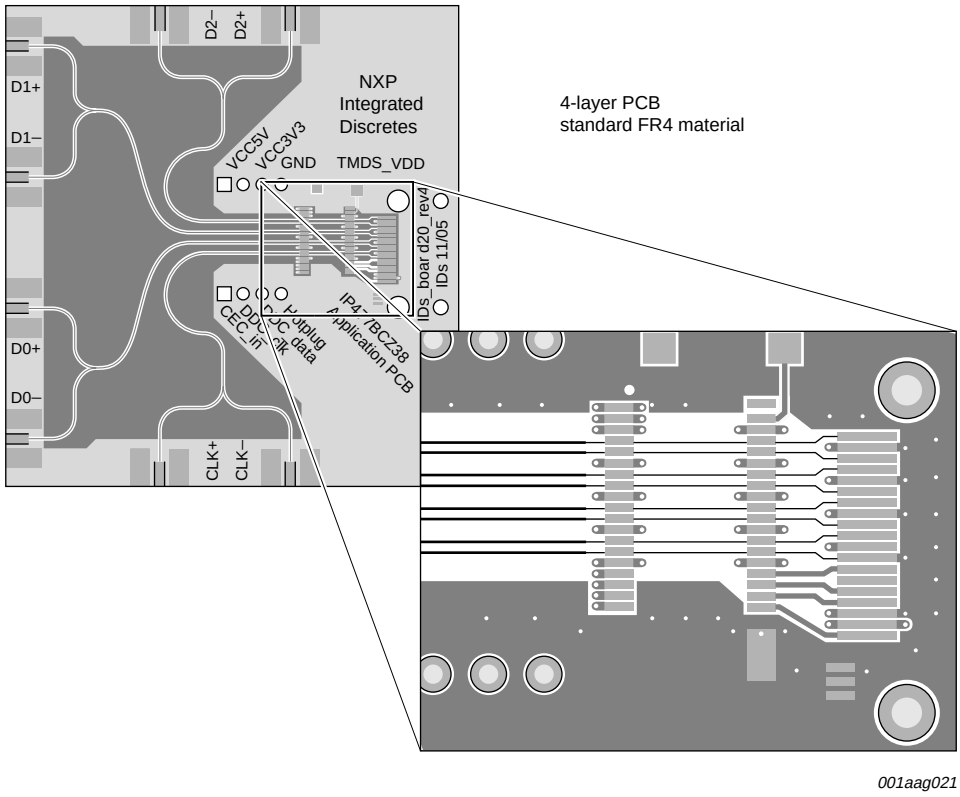


Fig 19. Reference board IP4776CZ38

The most effective way to design the TMDS lines is by using a field simulator. Based on the simulation results, a test PCB should be designed to compare the simulation results with a real PCB. The simulation can be optimized by using the parameters of the PCB material, which will differ from one PCB vendor to another. If a field simulator is not available, one test PCB can be made with different geometrical test structures to find the optimal design for this specific PCB material.

The NXP PCB recommendation was verified in the lab and in the HDMI compliance center at Caen (France) but be aware that the PCB material may differ from yours.

Experience shows that the PCB material has a major impact on the impedance of the micro strip lines. To evaluate the PCB material used and the number of layers, a test PCB can be made as shown in Figure 20.

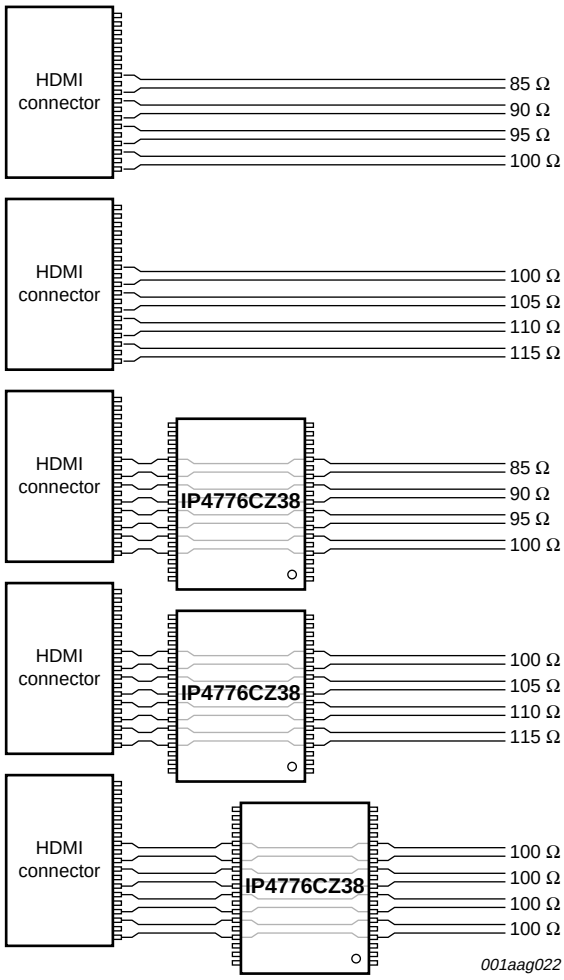


Fig 20. Test structure PCB (principles)

The first two structures without an IP4776CZ38 are used to verify the impedance of the micro strip lines. The next two structures will indicate what the impedance underneath the IP4776CZ38 has to look like in order to pass the HDMI compliance test. The last structure gives a good indication about the spread of the impedance and the device position.

Section 7.1 gives a principle description: the exact dimensions and positions are available as a Gerber file. The Gerber file of the test PCB will be made available upon request.

The impedance measurements need special equipment. For customers who do not have such equipment or require a second analysis result, we offer a TDR analysis of the PCB to ensure a pass at the HDMI-compliance test.

7.1 Geometry of micro strip lines (TMDS)

The design of a 100 Ω differential impedance has to be optimized for the PCB material and the number of layers. It is possible to calculate the impedance (Z_0) and the differential impedance (Z_{diff}) using the following equations (see also Figure 21).

$$\left(Z_0 = \frac{60}{\sqrt{0.457\varepsilon_r + 0.67}} \times ln\left(\frac{4h}{0.67(0.8W + t)}\right)\right)\ \Omega$$

$$Z_{diff} \approx 2Z_0\left(1 - 0.48e^{\left(-0.96\frac{S}{h}\right)}\right)\ \Omega$$

The results are valid up to a few GHz.

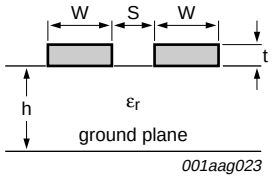


Fig 21. Geometrics for TMDS lines

Solid ground plane underneath the micro strip lines is part of the micro strip line design.

Table 3. Parameters for 2- and 4-layer PCB (FR4)

Parameter	4 layer	2 layer	Unit
Trace width (W)	5 (0.127)	8 (0.203)	mil (mm)
Spacing (S)	4 (0.102)	4 (0.102)	mil (mm)
Layer height (h)	4.5 (0.114)	63 (1.6)	mil (mm)
Relative permittivity (ε_r)	4.3	4.3	
Copper thickness (t)	1 (0.0254)	1 (0.0254)	mil (mm)
Z_{diff}	100.37	108.22	Ω

As an example, Table 3 shows all parameters which are necessary to design a 2-layer and a 4-layer board for a differential impedance (Z_{diff}) of 100 Ω.

Demonstration versions of simple simulator software are available on the internet to make the first steps.

7.2 TDR measurements of the IP4280CZ10

Prior to mass production of any licensed product or component that claims compliance with the HDMI specification, each adopter must test a representative sample for HDMI compliance. First, the adopter must self-test as specified in the HDMI compliance test specification. The HDMI compliance test specification provides a set of testing procedures and establishes certain minimum requirements. Such compliance testing is limited to evaluating the compliance of the application with the HDMI specification.

The compliance test specification was developed by the HDMI founders group to assist manufacturers in ensuring the compliance of their products with the HDMI specification. It consists of numerous tests designed to check for compatibility of various HDMI-related aspects of a product, including audio, video, EDID, electrical signaling, protocols, etc.

The test passes when the TDR curve is within the HDMI specification of 100 Ω ± 15 % (85 Ω to 115 Ω). The impact of ESD protection is reduced impedance caused by the capacitance of the ESD protection diode.

The TDR results show the impedance with respect to the geometric position. The HDMI connector is visible on the left side followed by the impact of the ESD protection device. The distance between the HDMI connector on the protection device influences the impact of both components. An inductive connector can partly compensate a capacitance impact of the protection device.

The signal flow is split up over the paths through the protection device and through the micro strip lines on the PCB.

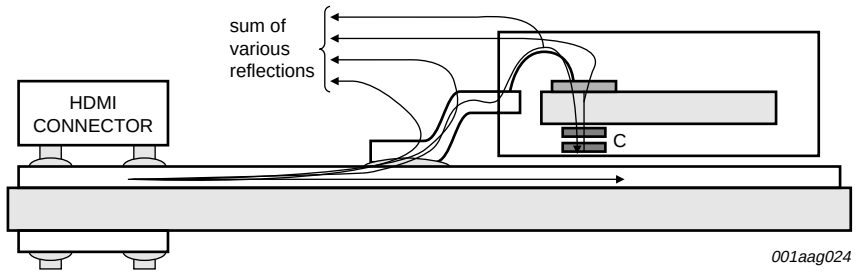


Fig 22. Signal flow on PCB and ESD protection device

The impact of the ESD protection device overlaps the impact of the signal track on the PCB. The impedance change in the TDR measurement graph can give the impression that the impact is behind the device because the length of the signal inside the device is longer than the signal track underneath the device. To compensate the impact of the ESD protection device, the impedance of the micro strip lines can have a higher value (110 Ω instead of 100 Ω), which is still within the impedance window of 85 Ω to 115 Ω to fulfill the HDMI specification.

The HDMI connector increases the impedance with an inductive load; the protection device reduces the impedance with a capacitive load. The distance between the HDMI connector and the protection device can fine-tune the impedance because of the mutual compensation of these inductive and capacitive loads.

8. ESD protection of HDMI transceivers requiring level shifting (IP4776CZ38)

The IP4776CZ38 is designed for DVI/HDMI interface protection. The IP4776CZ38 also includes level shifting and backdrive protection. Figure 23 shows the schematics of the IP4776CZ38 with all necessary and desirable interface isolation functions.

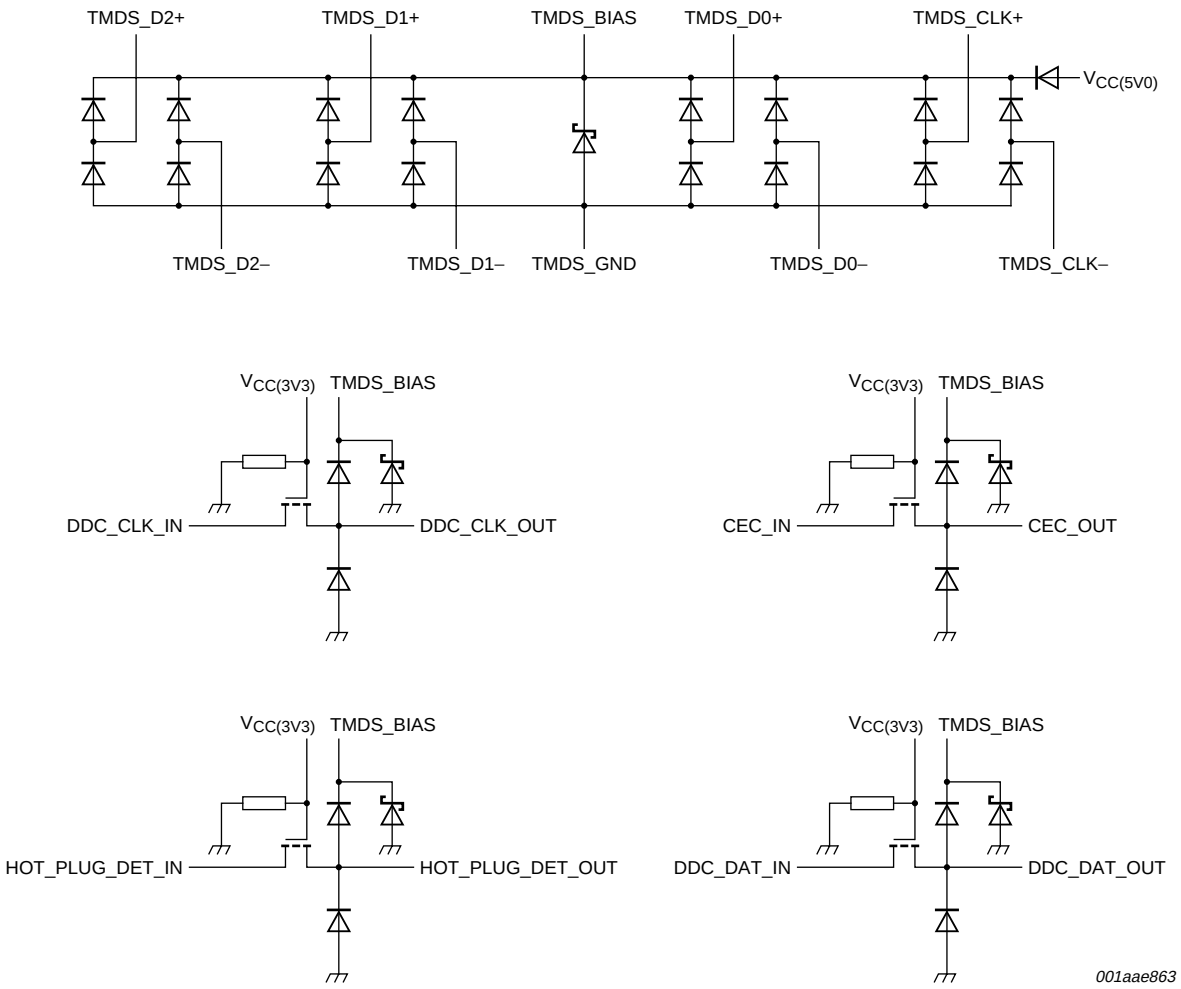


Fig 23. Schematics of the IP4776CZ38

Features of the IP4776CZ38:

- Pb-free and RoHS compliant
- Integrated high-level ESD protection, level shifting and backdrive protection
- All TMDS lines with integrated rail-to-rail clamping diodes with downstream ESD protection of ±8 kV contact according to IEC 61000-4-2, level 4 standard
- Matched 0.5 mm trace spacing
- Bidirectional level shifting N-channel FETs provided for DDC clock and DDC data channels
- TMDS lines with ≤ 0.05 pF matching of capacitance between the TMDS pairs
- Line capacitance < 1 pF per channel
- Backdrive protection
- Dedicated 38-pin TSSOP lead-free package for high-speed signals
- Compliant with HDMI 1.2 and HDMI 1.3 specification

One of the main advantages of such an integrated solution is that the IP4776CZ38 solution contains a high safety margin with respect to the HDMI TDR measurements compared to any discrete solutions.

With interfaces operating in the high frequency range, board routing becomes a critical factor that determines whether the system as a whole will pass or fail the HDMI-compliance tests. To be HDMI compliant, the channel impedance of the TMDS lines must be carefully tuned to 100 Ω ± 15 %.

The disadvantage of conventional ESD protection devices such as varistors or standard diodes is their relatively high capacitive load that either leads to failing of the HDMI-compliance tests or to significant routing difficulties and various board layouts to optimize the routing. As such, manufacturers have often used polymer-based protection devices which provide low line capacitance. The major disadvantage with these components is their high minimum breakdown voltage, in the range of 150 V and above, their degradation through ESD strikes, as well as their expense.

The IP4776CZ38 from NXP Semiconductors provides all advantages necessary for the HDMI interface and adds only very limited capacitive load comparable to polymer-based protection devices. This component has been successfully tested both by Silicon Image and NXP Semiconductors internal HDMI testing facility, and due to its very low line capacitance of 0.7 pF is also compliant with the HDMI 1.3 specification.

8.1 Application schematic and layout proposal (IP4776CZ38)

Figure 24 shows the IP4776CZ38 in the typical application schematic of an HDMI receiver port (HDMI sink). Figure 25 shows an HDMI transmitter port (HDMI source). The diagrams demonstrate the connector, the NXP Semiconductors device and the required external devices for the DDC, CEC and Hot-Plug signals.

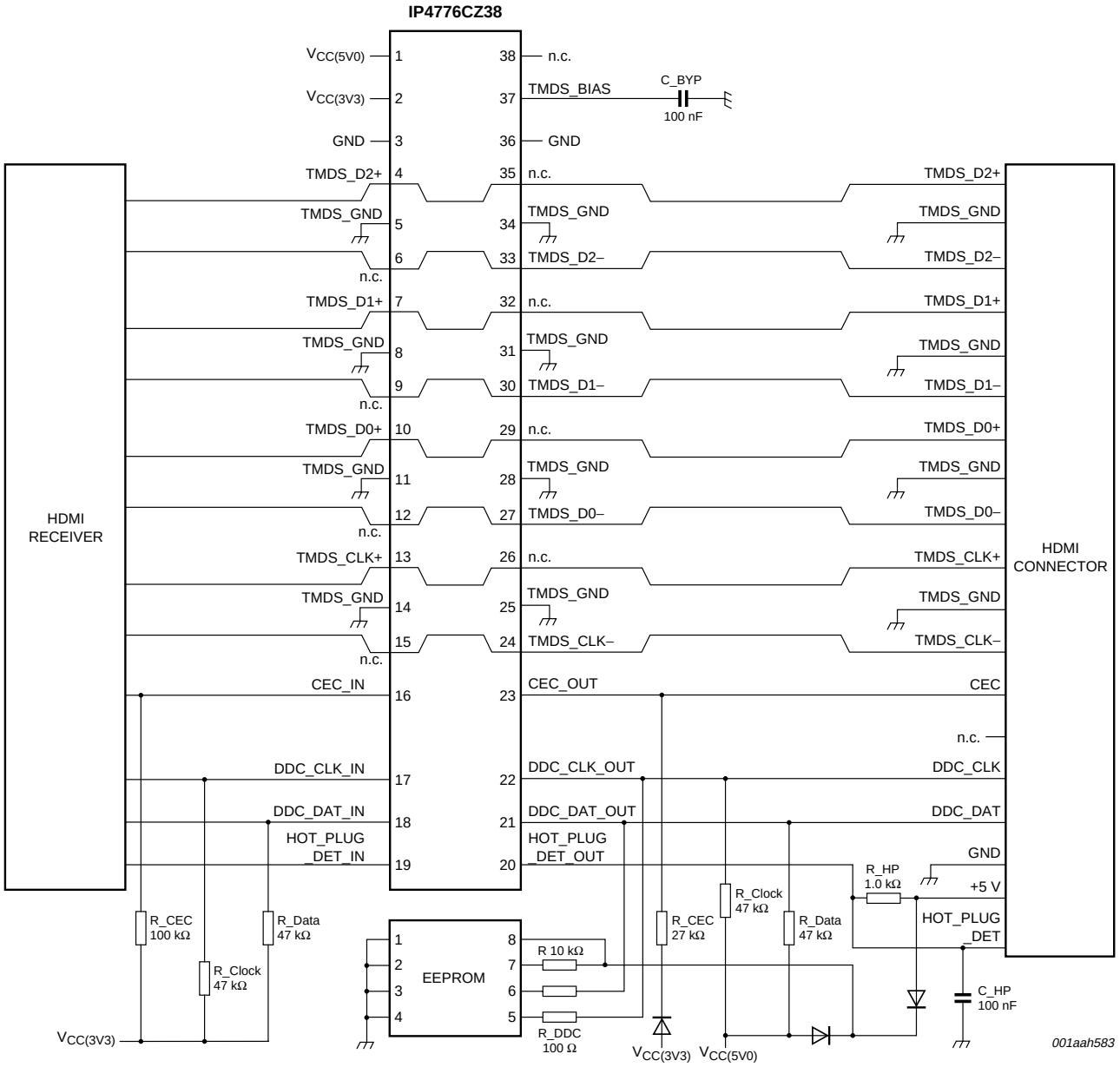


Fig 24. HDMI receiver

Figure 24 and Figure 25 show different configurations for using the IP4776CZ38 with an HDMI receiver or transmitter. The differences, which relate to the DDC, Hot-Plug and CEC lines, are explained in Section 4 “Level shifting” and Section 5 “Backdrive protection”. ESD protection and backdrive protection are used on the DDC, Hot-Plug and CEC lines. DDC and Hot-Plug lines also use level shifting. At the transmitter side an additional power limiter device is recommended to limit the 5 V current to 500 mA or less, in case of for example, a short of the HDMI connector.

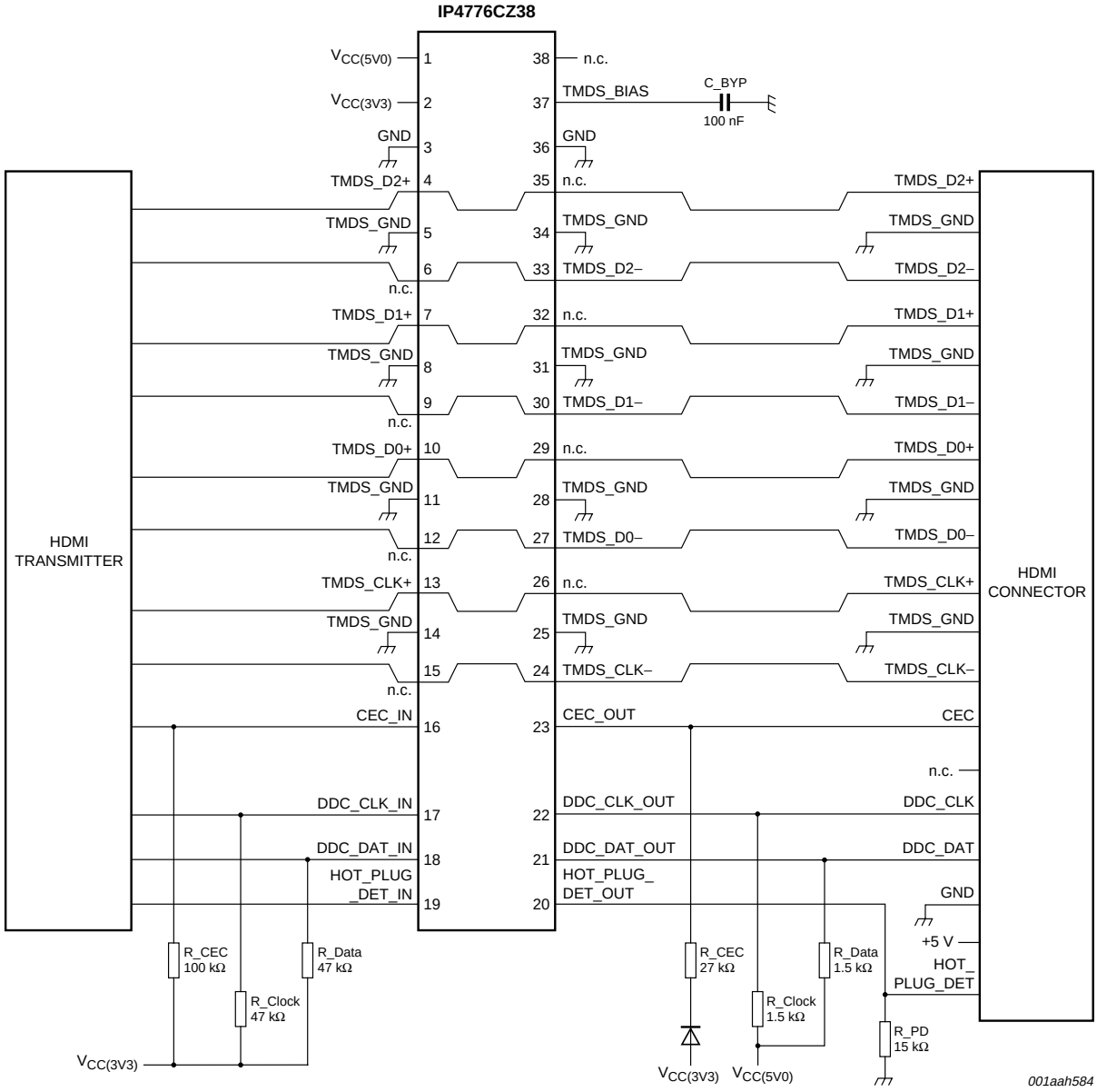


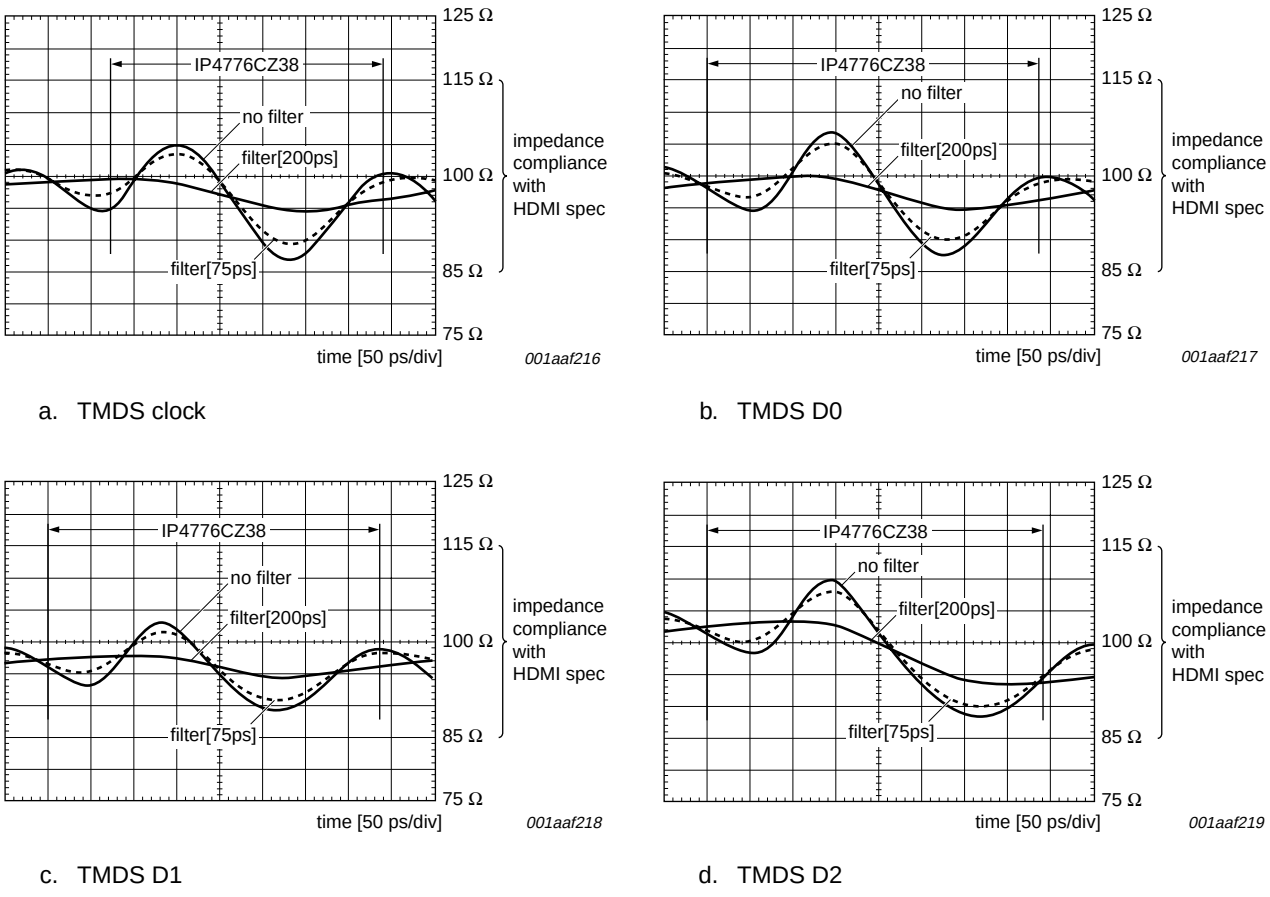
Fig 25. HDMI transmitter

For high-frequency applications like HDMI, an accurate layout is of similar importance to the electrical functionality of the devices (see Section 7 “PCB design”). The reason is that parasitic capacitance, inductance or mismatched impedance influence the input impedance, and the input impedance is a very sensitive parameter to fulfill the HDMI compliance test.

The IP4776CZ38 uses a TSSOP38 package, which makes this accurate layout for HDMI very simple. The IP4776CZ38 should be mounted close to the HDMI interface for maximum ESD protection efficiency. The choice of the package and the pinning chosen allows a straight routing of the TMDS lines through the package, thereby limiting potential parasitic inductance generated by complex routing.

8.2 TDR measurements (IP4776CZ38)

HDMI-compliance tests have been performed at NXP Semiconductors and Silicon Image compliance test centers. The compliance test specification requires the input impedance of the TMDS lines to be 100 Ω ± 15 Ω. To fulfill this requirement, the ESD protection device has to present a very low line capacitance. With the IP4776CZ38, NXP Semiconductors has achieved an ultra-low line capacitance of 0.7 pF typical. In order to demonstrate the excellent low line capacitance, TDR measurements were performed also at 75 ps and 35 ps (unfiltered) TDR step rise times, in addition to the standard 200 ps rise times. As shown in Figure 26, the IP4776CZ38 easily passes at 200 ps, 100 ps and even if 'no filter' condition is used. Due to the very low line capacitance of the IP4776CZ38, customers can use a more relaxed PCB design. Furthermore, this low line capacitance allows full compliance with the HDMI 1.3 specification.



a. TMDS clock

b. TMDS D0

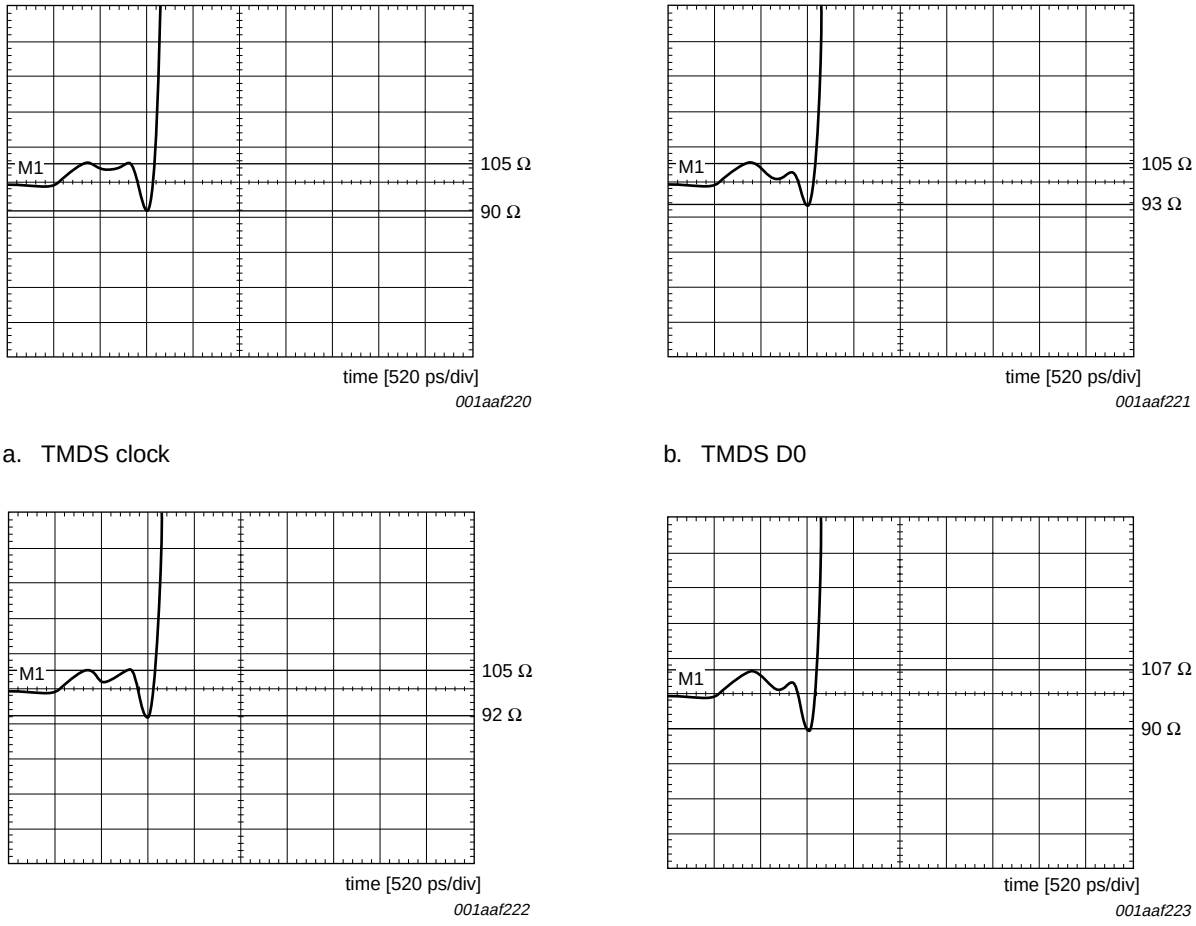
c. TMDS D1

d. TMDS D2

Fig 26. TDR measurements at NXP Semiconductors

The TDR step rise times were varied with mathematical filter options on the TDR equipment. The TDR measurements depicted in Figure 26 were performed at NXP Semiconductors and show the upper and lower HDMI specification limit indicated by lines at 115 Ω and 85 Ω. Clearly the IP4776CZ38 is well within the limits.

In addition to the TDR measurements at NXP Semiconductors, those at Silicon Image shown in Figure 27 show the highest and lowest impedance as measured for the IP4776CZ38. Also in these measurements, the IP4776CZ38 is well within the HDMI specification limits.



a. TMDS clock

b. TMDS D0

c. TMDS D1

d. TMDS D2

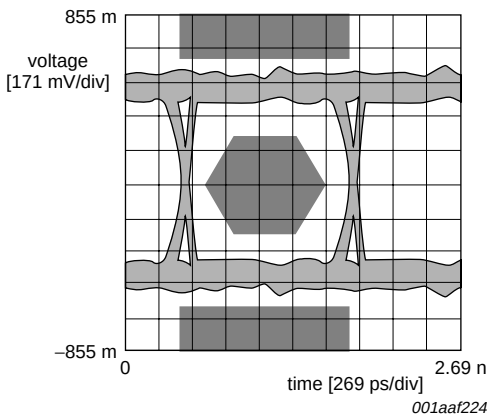
Fig 27. TDR measurements at Silicon Image

The step increase of the impedance shown at the right side is due to the open-end structure on the measurement board.

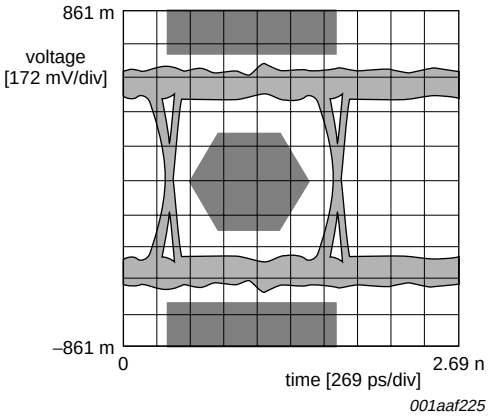
8.3 Eye diagram measurements (IP4776CZ38)

Another important measurement of the quality of the transmission signals are the Eye diagram measurements. The minimum eye opening is defined by the CTS octagons in Figure 28. Any ESD protection influences the signal due to the internal parasitic resistance and capacitance. For the high-frequency HDMI design, it is important that the ESD protection has a minimum parasitic capacitance to pass the HDMI specification. The Eye diagram measurements in Figure 28 were performed at NXP Semiconductors and show the influence of the IP4776CZ38. To demonstrate the parasitic influence, identical measurements have been performed with and without the IP4776CZ38 chip on the same

board. The measurement results underline a negligible increase of the data jitter by only 3.5 ps due to the parasitic impact of the IP4776CZ38. The IP4776CZ38 effectively has no impact on the Eye pattern.



a. Measured without IP4776CZ38



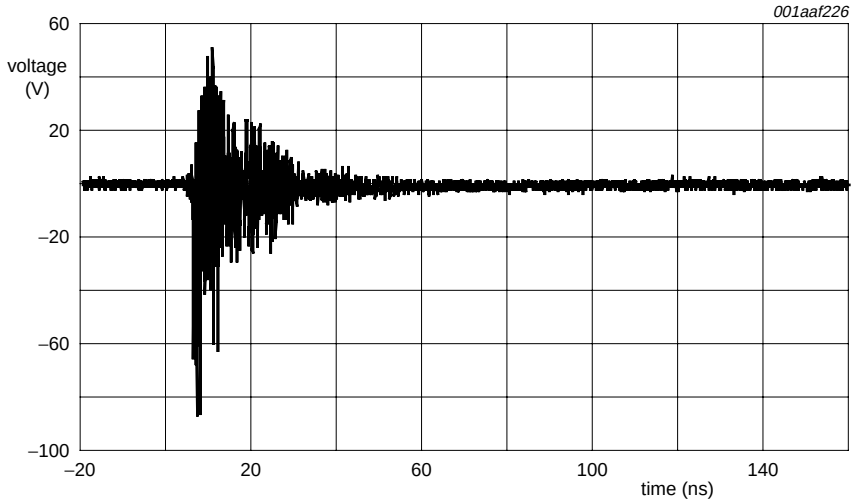
b. Measured with IP4776CZ38

Fig 28. Eye diagram measurements

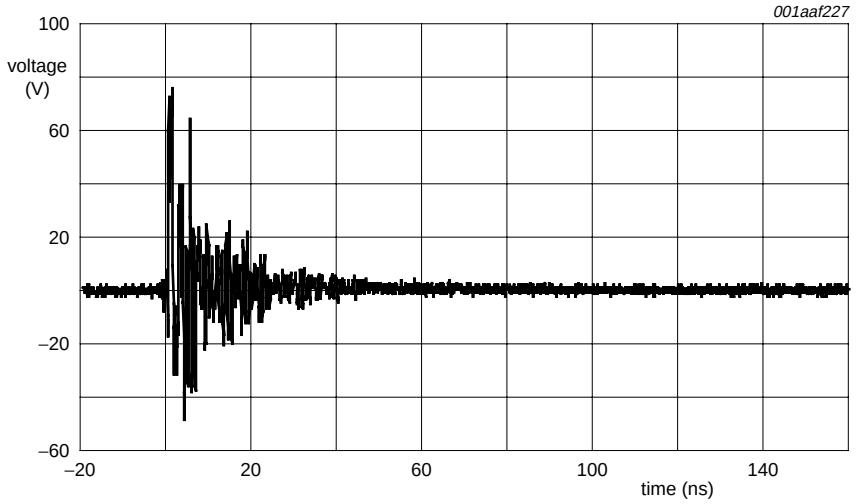
The signal frequencies at the TMDS lines (D0, D1 and D2) are about 10 times the pixel clock of the video signal. The frequency of the pixel clock depends on the video resolution selected. The minimum value is 25 MHz for PAL (720 × 576i) and NTSC (720 × 480i) at standard resolution with pixel repetition (250 MHz on TMDS lines). The maximum pixel clock is 74.25 MHz for HDTV (1920 × 1080i, 742.5 MHz on TMDS lines). The upcoming 1080p format will double the pixel clock frequency to 148.50 MHz (1.5 GHz at TMDS lines) and the new 10-bit color format will enhance the pixel clock frequency to about 200 MHz (2 GHz at TMDS lines).

8.4 Pulse clamping performance (IP4776CZ38)

Following the two ESD standards, HBM and IEC 61000-4-2, the clamping voltage of the TMDS lines is measured. The results of measurements shown in Figure 29 indicate a maximum clamping voltage of 18.2 V for the HBM and 37.6 V for IEC 61000-4-2 level 4. HDMI transceivers (standalone or integrated) typically have a 2 kV internal ESD protection. The low maximal clamping voltage of the IP4776CZ38 reduces the ESD strikes so that the total HDMI system easily survives high-energy ESD pulses according to the IEC 61000-4-2 level 4 standard.



a. ESD clamping example (IEC 61000-4-2 –8 kV)



b. ESD clamping example (IEC 61000-4-2 +8 kV)

Fig 29. Clamping voltages

9. Summary

For a high-speed interface such as DVI or HDMI, the use of high-level ESD protection is highly recommended. The cost of applications such as a digital TV or a Set-Top Box is simply too high to risk field returns. A fail can also damage company brand name and image. The continuous trend towards sub-micron CMOS processes at 120 nm, 90 nm, 65 nm and 45 nm technology nodes also contributes to a very high sensitivity of core ICs, making ESD protection mandatory.

The high-speed ESD protection devices discussed in this application note fully comply with both crucial requirements:

- The high-level ESD protection according to the international standards for consumer applications (IEC 61000-4-2 level 4)
- The ultra-low line capacitance requirement for the HDMI high-speed lines are fully achieved

The additional functions of level shifting and backdrive protection, integrated in an optimized package for HDMI applications, give the IP4776CZ38 an optimum level of integration. This package allows and supports optimal routing of the TMDS lines to minimize parasitic influences.

The NXP Semiconductors high-speed ESD protection devices are fully compliant with HDMI, and support easy routing and relaxed board layout at the highest protection levels. Therefore these devices are regarded as a protection standard of choice to be implemented on all new customer designs.

10. Abbreviations

Table 4. Abbreviations

Acronym	Description
ATC	Authorized Testing Center
CEC	Consumer Electronics Control
CTS	Compliance Test Specifications
DDC	Data Display Channel
DTV	Digital TeleVision
DUT	Device Under Test
DVD	Digital Versatile Disc
DVI	Digital Visual Interface
EDID	Extended Display Identification Data
ESD	ElectroStatic Discharge
FET	Field Effect Transistor
GPIO	General Purpose Input/Output
HBM	Human Body Model
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
HDTV	High-Definition TeleVision
IEC	International Electrotechnical Commission
I/O	Input/Output
MSL	Micro Strip Line
NMOS	n-type Metal-Oxide Semiconductor
NTSC	National Television Standards Committee
PAL	Phase Alternate Line
PCB	Printed-Circuit Board
RoHS	Restriction of the use of certain Hazardous Substances
RC	Resistor Capacitor
STB	Set-Top Box
TDR	Time Domain Reflection
TMDS	Transition Minimized Differential Signaling

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